REMARKS

Applicant gratefully acknowledges the allowance of claims 64-68 and the Examiner's indication of allowability for claims 51-53, 60-63, 72-74, and 78. No amendments to the claims are made. Claims 1-46 have been cancelled without prejudice to their underlying subject matter. Claims 47-78 are pending. Attached Appendix A includes a replacement FIG. 15 and shows amendments to the drawings.

Applicant responds to the Office Action's indication of reasons for allowance in relation to claims 64-68. The Office Action states that the references of record do not teach or suggest at least "a memory device comprising: at least one first epitaxial silicon stud with a silicide cap and at least one second epitaxial silicon stud without a silicide cap; and a conductive plug within said insulating sidewall and in electrical contact with said second epitaxial silicon stud." While Applicant generally agrees with this reasoning, Applicant respectively asserts that the prior art also fails to teach or suggest "at least one first epitaxial silicon stud with a silicide cap and at least one second epitaxial silicon stud without a silicide cap, each said stud in contact with a respective source and drain region of said at least one wordline gate" and "at least one bit line over and in electrical contact with said at least one first epitaxial silicon stud and partially overlying said at least one second epitaxial silicon stud, but electrically isolated therefrom by an insulating sidewall," as recited by independent claim 64. It is not merely the contact plug in electrical contact with the second stud that makes the claims patentable; these claims are patentable for this reason also.

The drawings stand objected to under 37 C.F.R. § 1.83(a) as not showing every feature of the invention claimed. Applicant respectfully traverses this objection.

The Office Action indicates that no drawing shows "an interconnect line . . . in electrical contact with said first conductive stud (i.e., claim 1)." This feature of the claim(s) is shown in, for example, FIG. 15 where the first conductive stud (22a) is shown to be in electrical contact with the overlying interconnect line (26) through the cap (24) over the stud (22a) (although the cap is absolutely necessary). Although not believed necessary, Applicant submits a replacement FIG. 15, which adds a reference "26" to more clearly label the interconnect line (26) in electrical connection with contact stud (22a). Mark-up and clean versions of this replacement drawing are attached at Appendix A, with changes shown in red. No new matter is added.

The Office Action also indicates that in FIG. 16, which shows a cross section of the structure of FIG. 15 through line XVI-XVI, the interconnect line (26) is insulated from both conductive studs (22b). This is correct because FIG. 16 shows how some studs (22b) are so insulated from the overlying contact line (26), which is electrically connected to an adjacent contact stud (22a), as shown in FIG. 15.

FIG. 16 is also objected to because it allegedly has a cross-section not corresponding with the line XVI-XVI of FIG. 15. The line XVI does indeed correspond to the drawing of FIG. 16; it passes through the middle of the drawing of FIG. 15. Because of the perspective view shown in FIG. 15, the line does, however, bisect the location of the contact stud (22b) as shown in FIG. 16. It is the same cross-section line as shown in FIG. 1 (i.e., line II-II). The replacement FIG. 15 shifts the position of the contact (36) slightly to make this more clear.

In view of the above and based on the replacement drawing submitted herewith, Applicant respectfully requests that the objection to the drawings be withdrawn.

Claim 47 stands rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,705,838 ("Jost et al."). Applicant respectfully traverses this rejection.

Claim 47 defines a memory device and recites "a first conductive stud and a second conductive stud" and "an interconnect line over and in electrical contact with said first conductive stud, wherein a portion of said interconnect line overlays a portion of said second conductive stud" and "an insulating sidewall separating said interconnect line from said second conductive stud." Such a device is not disclosed by Jost et al.

The Office Action indicates that Jost et al. discloses each and every element of claim 47 in that it discloses a semiconductor memory device comprising a conductive layer (36; assumedly alleged to be a first conductive stud), a conductive layer (38; assumedly alleged to be a second conductive stud), a bit line (55; assumedly alleged to be an interconnect line over and in electrical contact with said first conductive stud, where a portion of said interconnect line overlays a portion of said second conductive stud), and a dielectric layer (40; assumedly alleged to be an insulating sidewall separating said interconnect line from said second conductive stud). This interpretation of Jost et al. is incorrect.

The Office Action indicates that the ONO cell dielectric layer (40), which is specifically disclosed by Jost et al. to be a capacitor dielectric (FIG. 5 and col. 5, ll. 58-60), is in fact an "insulating sidewall separating said interconnect line from said second conductive stud," as recited by claim 47. This is incorrect. The capacitor dielectric (40) is <u>not</u> an insulating <u>sidewall</u> as claimed, as discussed in the present application's specification, and as such terminology is commonly used in the art. Feature 40 of Jost et al. is a <u>capacitor dielectric</u> used to separate the two conductive capacitor plates (features

38 and 42) and in no way resembles a "sidewall." Additionally, even if this capacitor dielectric (40) of Jost et al. could be considered a sidewall, which it cannot, it does not separate an interconnect line from a conductive stud as is clearly shown by FIG 5 of Jost et al. The alleged conductive stud (i.e., capacitor storage node 38) of Jost et al. is not separated from the alleged interconnect line (i.e., bit line 55) by this capacitor dielectric (40). As stated above, this capacitor dielectric (40) separates the feature alleged in the Office Action to be a conductive stud (capacitor storage node 38) from an overlying capacitor plate (42) feature, not the bit line (55) indicated in the Office Action to be the interconnect line. There is no "insulating sidewall separating said interconnect line from said second conductive stud" disclosed anywhere by Jost et al. and claim 47 is not anticipated by Jost et al. for this reason.

Additionally, the Office Action states that Jost et al. discloses "a first conductive stud and a second conductive stud" and "an interconnect line over and in electrical contact with said first conductive stud, wherein a portion of said interconnect line overlays a portion of said second conductive stud." It does not. Jost et al. at least fails to disclose "a second conductive stud" in such a configuration The ONO cell (capacitor) dielectric layer (40) disclosed by Jost et al. is not a "conductive stud" as the term is used in the claim, in the application's specification, or in the art; it is a capacitor plate. No such "second conductive stud" is shown in any figure of Jost et al., including FIG. 5, or discussed in its specification. Feature 38 of Jost et al. alleged to be the second conductive stud recited by claim 47 is specifically disclosed by Jost et al. at col. 4, ll. 4-7 to be a capacitor storage node, i.e., a capacitor plate, not a "stud" of any kind. For this reason, also, independent claim 47 is not anticipated by Jost et al.

To establish a *prima facie* case of anticipation, each and every element of the claim. M.P.E.P. § 2131 (citing Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)). **"The identical invention must be shown in as complete detail as is contained in the ... claim."** Id. (quoting Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)) (emphasis added). **The elements must be arranged as required by the claim.** Id. (citing In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)) (emphasis added).

Here, the Office Action fails to make a *prima facie* case for anticipation of independent claim 47 since it does not indicate that Jost et al. discloses the positioning of the dielectric layer/insulating sidewall is as claimed (i.e., "separating said interconnect line from said second conductive stud") and does not indicate that the reference discloses the positioning of the interconnect line with respect to the second contact stud is as claimed (i.e., "a portion of said interconnect line overlays a portion of said second conductive stud"). The Office Action has failed to indicate that the prior art discloses the identical invention in as complete detail as recited by the claim and has failed to indicate that the elements discussed as disclosed in the prior art are arranged as required by the claim. The Office Action fails to make a *prima facie* case of anticipation because it cannot do so; the reference simply does not anticipate the claim. The failure to state a *prima facie* case for anticipation provides additional reasoning that claim 47 is patentable over the cited art.

Since claim 47 is not anticipated by Jost et al., this independent claim, as well as each claim depending therefrom, is patentable over Jost et al. Further, no *prima facie* case has been established that Jost et al. anticipates claim 47. Applicant respectfully requests that the 35 U.S.C. § 102(b) rejection of claim 47 be withdrawn.

Claims 48-50 and 54-59 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Jost et al. in view of U.S. Patent 6,188,112 ("Bryant") and U.S. Patent 6,069,060 ("Matsumoto"). Applicant respectfully traverses this rejection.

Claims 48-50 and 54-57 depend from independent claim 47, which, as discussed above, is patentable over Jost et al. Regardless of what Bryant and Matsumoto disclose regarding the use of epitaxial silicon in memory devices, the subject matter for which they are cited in the Office Action, these references cannot supplement Jost et al. to remedy this primary reference's deficiencies with regard to the subject matter recited by claim 47 and missing from Jost et al. Like Jost et al., neither Bryant nor Matsumoto teaches or suggests "an interconnect line over and in electrical contact with said first conductive stud, wherein a portion of said interconnect line overlays a portion of said second conductive stud" and "an insulating sidewall separating said interconnect line from said second conductive stud," as recited by independent claim 47. Additionally, they do not teach or suggest the "second contact stud" recited by claim 47 and its position with respect to other features of the claimed subject matter. Therefore, independent claim 47 and dependent claims 48-50 and 54-57 are patentable over Jost et al., Bryant, and Matsumoto because the combined references do not teach each and every limitation of the claims.

Since claims 58-50 and 54-57 are patentable over Jost et al., Bryant, and Matsumoto, Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claims 48-50 and 54-57 be withdrawn.

Claim 58 defines a DRAM cell structure and recites "an access transistor with source and drain areas" and "a first conductive epitaxial silicon stud and a second conductive epitaxial silicon stud each in contact with a respective one of said source

and drain areas of said access transistor" and "a bit line over and in electrical contact with said first conductive epitaxial silicon stud, wherein at least a portion of said bit line overlays a portion of said second conductive epitaxial silicon stud" and "an insulating sidewall structure separating said bit line from said second conductive epitaxial silicon stud." This claimed device is not taught or suggested by Jost et al., Bryant, and Matsumoto.

As discussed above in relation to the patentability of independent claim 47 and the claims depending therefrom, none of Jost et al., Bryant, and Matsumoto teaches or suggests "a bit line over and in electrical contact with said first conductive epitaxial silicon stud, wherein at least a portion of said bit line overlays a portion of said second conductive epitaxial silicon stud" and "an insulating sidewall structure separating said bit line from said second conductive epitaxial silicon stud," as recited by claim 58. Also, these references fail to teach or suggest the "second contact stud" as recited by the claim. The failure of these references to disclose such subject matter has been discussed at length above in relation to the patentability of independent claim 47 and the claims depending therefrom. Therefore, for at least the same reasoning set forth above, independent claim 58 and dependent claim 59 are patentable over the cited references. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claims 58 and 59 be withdrawn.

Claims 69-71 and 75-77 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Jost et al. in view of Bryant and Matsumoto and also in view of U.S. Patent 6,051,509 ("Tsuchiaki"). Applicant respectfully traverses this rejection.

Claim 69 defines a processor-based system having a processor and a memory circuit and recites "a first conductive epitaxial silicon stud and a second conductive

epitaxial silicon stud" and "an interconnect line over and in electrical contact with said first conductive stud, wherein a portion of said interconnect line overlays a portion of said second conductive epitaxial silicon stud" and "an insulating sidewall structure separating said interconnect line from said second conductive epitaxial silicon stud." Such a device is not taught or suggested by Jost et al., Bryant, Matsumoto, and Tsuchiaki.

As discussed above in relation to the patentability of independent claim 47 and the claims depending therefrom, and again in relation to claim 58 and its depending claims, none of Jost et al., Bryant, and Matsumoto teaches or suggests "an interconnect line over and in electrical contact with said first conductive stud, wherein a portion of said interconnect line overlays a portion of said second conductive epitaxial silicon stud" and "an insulating sidewall structure separating said interconnect line from said second conductive epitaxial silicon stud," or the "second contact stud," as recited by claim 69. Tsuchiaki cannot remedy these deficiencies because it likewise fails to teach or suggest such subject matter. Therefore, for at least the same reasoning set forth above for other independent claims (i.e., claims 47 and 58), independent claim 69 and dependent claims 70, 71, and 75-77 are patentable over the cited references. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claims 69-71 and 75-77 be withdrawn.

Applicant believes all pending claims are in immediate condition for allowance and respectfully requests a Notice of Allowance for all pending claims (47-78).

Dated: November 30, 2005

Respectfully submitted,

By_____

Thomas J. D'Amico
Registration No.: 28,371
Ryan H. Flax
Registration No.: 48,141
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorney for Applicant

APPENDIX A

Amendments to the drawings:
Replacement FIG. 15
(mark-up and clean versions)

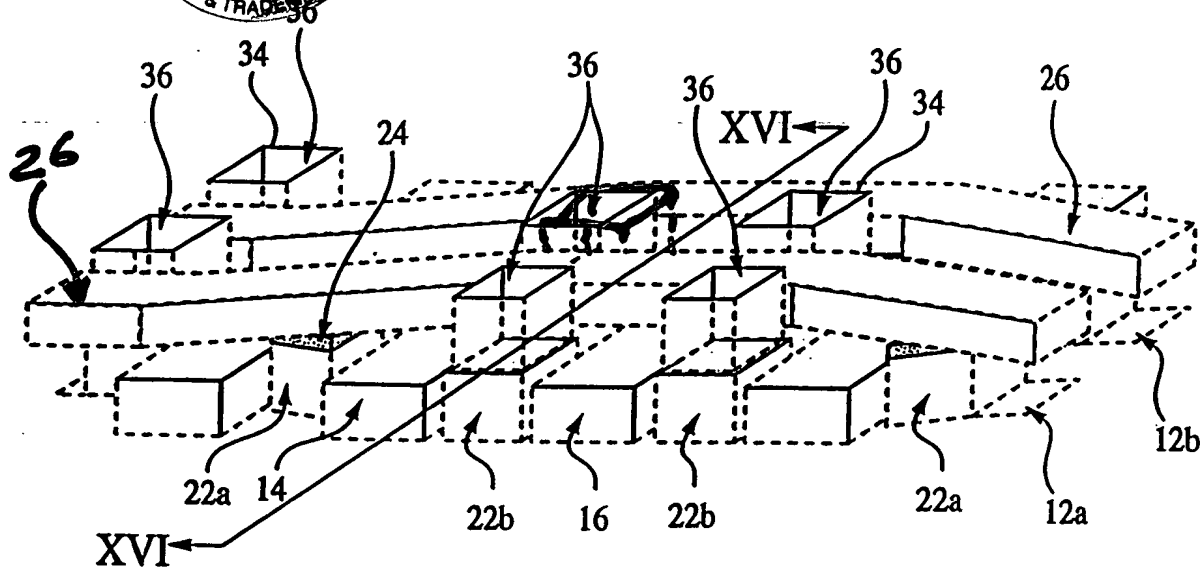

FIG. 15

MARK-UP

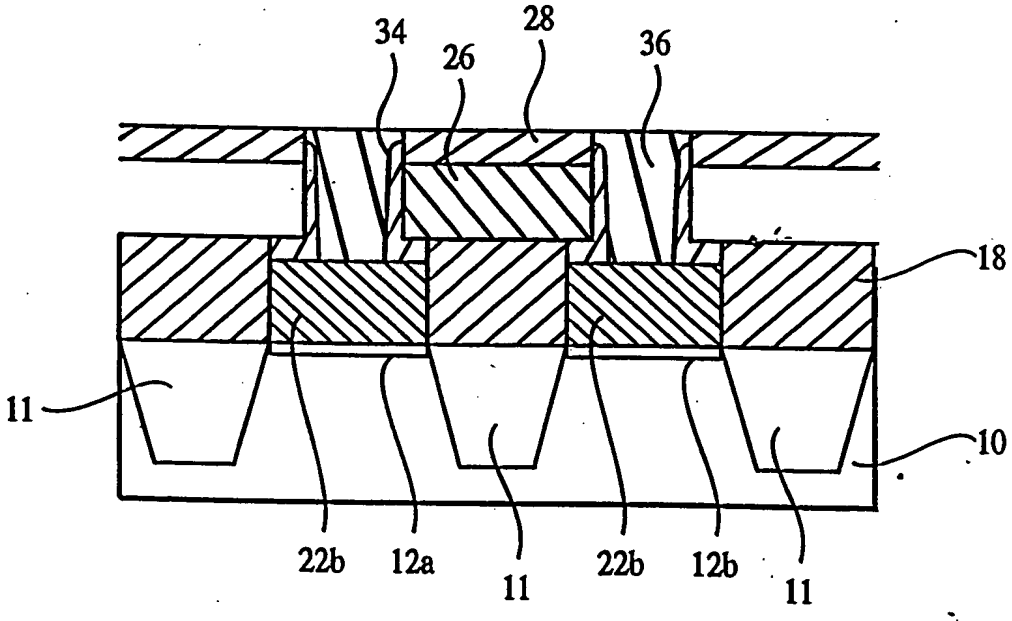

FIG. 16